What is Claimed is:

[c1] A structure formed on a substrate comprising:
a plurality of isolation filled trenches in the substrate;
a plurality of holes in the substrate, each having a plurality of sidewalls and a bottom wall, located in a region of a semiconductor substrate in which said plurality of isolation filled trenches are absent, said holes having a depth proximate that of said plurality of isolation filled trenches;
insulating material present in each of said plurality of holes on said plurality of sidewalls and bottom wall; and
a conductor overfilling each of said holes and extending onto an adjacent upper surface of the substrate.

[c2] The structure of Claim 1 further comprising counter-doped regions present in pillar areas of said semiconductor substrate that surround said holes.

[c3] The structure of Claim 1 further comprising well implants regions located in said semiconductor substrate.

[c4] The structure of Claim 1 further comprising at least one transfer device located atop a surface of said semiconductor substrate adjoining said plurality of holes.

[c5] The structure of Claim 4 wherein said at least one transfer device is a field effect transistor.

[c6] The structure of Claim 2, wherein said insulating material is thicker on said bottom walls of said plurality of holes than on said plurality of sidewalls of said plurality of holes.

[c7] The structure of Claim 6, wherein said insulating material is disposed on said upper surface of the substrate beneath portions of said conductor thereon.

[c8] The structure of Claim 1, wherein said holes have a depth greater than said plurality of isolation-filled trenches.

[c9] The structure of Claim 8, wherein an isolation dopant region is disposed below said bottom walls of said plurality of holes.

[c10] The structure of Claim 1, wherein the substrate has a buried insulation region, and wherein said plurality of holes extend into said buried insulation region.

[c11] A method of fabricating a capacitor structure comprising the steps of:
forming a plurality of holes in a region of a semiconductor substrate, each hole having a plurality of sidewalls and a bottom wall;
forming insulating material in each hole, wherein in first ones of said holes said insulating material completely fills said holes and in second ones of said holes said insulating material formed only on said plurality of sidewalls and said bottom wall; and
overfilling each of said second ones of said hole with a conductor.

[c12] The method of Claim 11 further comprising forming counter-dopant regions in said substrate prior to said filling step.

[c13] The method of Claim 11 further comprising forming a transfer device adjoining said plurality of holes.

[c14] The method of Claim 11 wherein said counter-dopant regions are formed using an angled implant process.

[c15] The method of Claim 11, wherein said step of forming said insulating material in each hole further comprises the steps of:
filling all of said holes with a first insulator;
masking said first ones of said holes;
etching a portion of said first insulator from said second ones of said holes; and
forming a second insulator on exposed portions of said plurality of sidewalls of said second ones of said holes.

[c16] The method of Claim 11, wherein said step of etching a portion of said first insulator is a timed etch.

[c17] The method of Claim 11, wherein said insulating material in said second ones of said holes is thicker on said bottom walls than on said plurality of sidewalls.

[c18] The method of Claim 11, wherein said holes have a depth greater than said plurality of isolation-filled trenches.

[c19] The method of Claim 18, wherein an isolation dopant region is disposed below said bottom walls of said plurality of holes.

[c20] The method of Claim 11, wherein the substrate has a buried insulation region, and wherein said plurality of holes extend into said buried insulation region.